APPARATUS AND METHOD FOR CONVERTING SINGLE-ENDED SIGNALS TO A DIFFERENTIAL SIGNAL, AND TRANSCEIVER EMPLOYING SAME

INCORPORATION BY REFERENCE OF RELATED APPLICATIONS

[0001] The present application is related to U.S. Patent Application Serial No. 09/629092, entitled "Active Resistive Summer for a Transformer Hybrid," filed July 31, 2000, and to U.S Patent Application Serial No. [not yet assigned], entitled "Active Resistive Summer for a Transformer Hybrid," filed concurrently herewith, both of which name Pierte Roo (the inventor of the present invention) and Sehat Sutardja as inventors, and each of which is hereby incorporated herein by reference.

BACKGROUND

1. Field of the Invention

[0002] The present invention relates generally to communication circuitry and, more particularly, to a method and apparatus for use in a communication circuit, such as an Ethernet or other network transceiver, for converting single-ended signals to a differential signal.

2. Related Art

[0003] In communication transceivers, and particularly in Ethernet transceivers which are capable of transmitting and receiving data at 1000 megabits bits per second,

communication is possible in a full-duplex mode. In other words, transmitting and receiving of data can occur simultaneously on a single communication channel. Implementation of such a full-duplex communication channel results in a composite signal (V_{TX}) being present across the output terminals of the transceiver, the composite signal V_{TX} having a differential transmission signal component and a differential receive signal component. In such a communication channel, the received signal (V_{RCV}) is derived by simply subtracting the transmitted signal (V_T) from the composite signal V_{TX} that is present at the transceiver output terminals. Hence, $V_{RCV} = V_{TX} - V_T$.

[0004] This subtraction can be accomplished by generating a signal (referred to as a replica signal) which substantially replicates the transmitted signal, and canceling or subtracting the generated replica signal from the composite signal V_{TX} at the output terminals of the transceiver. However, the replica signal is generated as two single-ended voltages, such as V_{TXR+} and V_{TXR-}, whereas the composite signal present at the output terminals of the transceiver is a differential signal. Consequently, in order to cancel the replica signal from the composite signal to thereby obtain the received signal, the two single-ended voltage signals must first be converted to a differential signal that can then be subtracted from the composite signal. This conversion, however, requires additional circuitry which adds to the cost and complexity of the transceiver.

SUMMARY

[0005] The present invention relates to a method and apparatus for converting the single-ended voltage signals in an Ethernet transceiver into a differential voltage signal, so that the differential voltage signal can be subtracted from the composite signal to produce an accurate receive signal.

[0006] According to one aspect of the present invention, a communication circuit is provided for an Ethernet transceiver. The communication circuit preferably includes a first sub-circuit having a first input which receives a composite differential signal including first and second differential signal components, a second input which receives a differential replica transmission signal, and an output which provides a differential receive signal which comprises the composite differential signal minus the differential replica transmission signal. The communication circuit also may include a second sub-circuit which produces first and second single-ended replica transmission signals which together substantially comprise a replica of the first differential signal component of the composite differential signal and a third sub-circuit, which is coupled to the first and second sub-circuits, and which produces the differential replica transmission signal from the first and second single-ended replica transmission signals.

[0007] The communication circuit may further include a fourth sub-circuit which is coupled to the first sub-circuit and which produces a time-shift between the first differential signal component of the composite differential signal and the second

differential signal component of the composite differential signal. The fourth sub-circuit may comprise a delay circuit which introduces a delay in the first differential signal component relative to the second differential signal component and, more particularly, may introduce a predetermined delay in the differential replica transmission signal relative to the first and second single-ended replica transmission signals from which the differential replica transmission signal is produced. The delay introduced by the fourth sub-circuit preferably substantially matches the predetermined delay introduced by the third sub-circuit. Also preferably, the first and second single-ended replica transmission signals are Class B signals, and the differential replica transmission signal is preferably produced from the first and second single-ended Class B replica transmission signals with a single operational amplifier.

[0008] According to another aspect of the invention, a communication circuit for an Ethernet transceiver includes: summing means having a first input for receiving a composite differential signal including first and second differential signal components, a second input for receiving a differential replica transmission signal, and an output for providing a differential receive signal which comprises the composite differential signal minus the differential replica transmission signal; replicating means for producing first and second single-ended replica transmission signals which together substantially comprise a replica of the first differential signal component of the composite differential signal; and converting means coupled to the summing means and the replicating means

for producing the differential replica transmission signal from the first and second single-ended replica transmission signals.

[0009] According to yet another aspect of the present invention, in an Ethernet transceiver a composite differential signal including first and second differential signal components is received at a first input, a differential replica transmission signal is received at a second input, the composite differential signal and the differential replica transmission signal are combined to thereby provide at an output a differential receive signal which comprises the composite differential signal minus the differential replica transmission signal. The differential replica transmission signal is developed from first and second single-ended replica transmission signals, which together substantially comprise a replica of the first differential transmission signal component of the composite differential signal.

BRIEF DESCRIPTION OF THE DRAWING

[0010] **FIG. 1** is a high-level schematic diagram illustrating a communication channel in connection with which the method and apparatus of the present invention may be used;

[0011] **FIG. 2** is a detailed schematic diagram illustrating one embodiment of a transceiver according to the principles of the present invention; and

[0012] **FIG. 3** is a detailed schematic diagram illustrating a second embodiment of a transceiver according to the principles of the present invention.

DETAILED DESCRIPTION

[0013] While the present invention will be described with respect to an Ethernet controller card for use in general purpose computers, printers, routers, etc. it is to be understood that the present invention may find applicability in other fields such as Internet communications, telecommunications, or any processor-to-processor applications using full-duplex communication. Also, rather than being embodied in discrete card, the method and apparatus of the present invention alternatively may advantageously be incorporated directly into a computer "mother board" or any other suitable hardware configuration, if desired.

[0014] Communication in an Ethernet computer network is illustrated in **FIG. 1**. As shown, an Ethernet communication channel 40 comprises a first Ethernet transceiver 42, a second Ethernet transceiver 44, and a two-wire interconnection 46 between the first Ethernet transceiver 42 and the second Ethernet transceiver 44. For example, the two-wire interconnection 46 may comprise a single twisted-pair of a Category 5 cable in accordance with IEEE gigabit transmission standard No. 802.3ab. As the Ethernet transceivers 42 and 44 may be substantially identical, only one of them is described herein.

[0015] The Ethernet transceiver 42 has a controlled current source 48, which is used to inject into the Ethernet transceiver 42 a control current I_{TX}, which corresponds to a signal to be transmitted from the Ethernet transceiver 42 to the Ethernet transceiver 44. Ethernet transceiver 42 also has a termination resistance 50 and a first coil 52 of a center-tap transformer 54. The center-tap transformer 54 also has a second coil 56 coupled to the two-wire interconnection 46 to provide signals transmitted by the first Ethernet transceiver 42 to the second Ethernet transceiver 44. The center-tap transformer 54 serves to couple AC voltage signals between the Ethernet transceivers 42 and 44 while effectively decoupling the Ethernet transceiver 42 from the Ethernet transceiver 44 with respect to DC voltage signals. A pair of terminals 58, 60 is provided to measure a voltage V_{TX} present across the resistor 50 as a result of both signals transmitted by the Ethernet transceiver 42 and signals received by the Ethernet transceiver 42 from the Ethernet transceiver 44 via the two-wire interconnection 46. The voltage V_{TX} thus comprises a composite differential signal that includes a differential transmission signal component and a differential receive signal component.

[0016] As described in more detail below, the differential receive signal component of the composite differential signal V_{TX} is determined in accordance with the present invention by subtracting a replica of the differential transmission signal component from the composite differential signal V_{TX}. In the illustrated embodiment, the Ethernet transceiver 42 includes the termination resistance 50, the center-tap transformer 54, and

an integrated circuit 62 containing communications circuitry for implementing the functionality of the Ethernet transceiver 42.

[0017] An exemplary embodiment of such Ethernet transceiver communications circuitry is illustrated in the schematic of **FIG. 2**. As shown in **FIG. 2**, an integrated circuit 70 has a pair of output terminals 72, 74, which are coupled to terminals 76, 78, respectively, of the winding 52 of the center-tap transformer 54. Current in the winding 52 of the center-tap transformer 54 induces a proportional current in the secondary winding (not shown in **FIG. 2**) of the center-tap transformer 54, and that proportional current is communicated over the two-wire interconnection 46 (**FIG. 1**) to another Ethernet transceiver coupled thereto. Also coupled between the output terminals 72, 74 is a termination resistance 80, which, in the illustrated embodiment of **FIG. 2**, comprises a pair of termination resistors 82, 84. Preferably, the termination resistors 82, 84 have resistance values to substantially match the 100 ohm characteristic impedance of Category 5 cable in accordance with established standards for Ethernet connections.

[0018] The integrated circuit 70 also includes a transmission signal replicator 86 or other suitable circuitry for generating first and second single-ended replica transmission signals V_{TXR+} and V_{TXR-}, which together substantially comprise a replica of the differential transmission component of the composite differential signal V_{TX}. In the illustrated embodiment, the transmission signal replicator 86 comprises a pair of metal-oxide semiconductor (MOS) transistors 88, 90.

[0019] The transistor 88 is coupled between the output terminal 72 and one end of a resistor 92, the other end of the resistor 92 being coupled to ground. Similarly, the transistor 90 is coupled between the output terminal 74 and one end of a resistor 94, the other end of which is coupled to ground. The gate of each transistor 88, 90 is coupled to and driven by the output of a respective operational amplifier 96, 98. The operational amplifier 96 has a non-inverting input 100 and an inverting input 102. The inverting input 102 of the operational amplifier 96 receives a feedback signal from the junction of the source of the transistor 88 and the resistor 92. Likewise, the operational amplifier 98 has a non-inverting input 104 and an inverting input 106, which receives a feedback signal from the junction of the source of the transistor 90 and the resistor 94.

[0020] A differential control voltage signal is applied between the non-inverting input 100 of the operational amplifier 96 and the non-inverting input 104 of the operational amplifier 98. This differential control voltage signal, when subjected to the voltage-to-current conversion brought about by the transmission signal replicator 86, provides the differential transmit signal component at the output terminals 72, 74. The feedback signal to the inverting input 102 of the operational amplifier 96 comprises a first single-ended replica transmit signal V_{TXR+}, and the feedback signal to the inverting input 106 of the operational amplifier 98 comprises a second replica transmit signal V_{TXR-}.

[0021] The single-ended replica transmit signals V_{TXR+} and V_{TXR-} are converted to a differential replica transmit signal by a converter circuit 107, which comprises respective

differential operational amplifiers 108, 110, each provided with suitable input and feedback resistors, as shown in **FIG. 2**. The outputs of the differential operational amplifiers 108 and 110 are coupled to a differential active summer 112, which, in the embodiment of **FIG. 2**, comprises a differential operational amplifier 114 with feedback resistors 116, 118.

[0022] Because the differential operational amplifiers 108 and 110 introduce a delay into the replica transmissions signals V_{TXR+} and V_{TXR-}, the composite differential signal V_{TX} is coupled to the differential active summer 112 through a further differential operational amplifier 120 arranged in a unity-gain configuration, with input resistors 122, 124, output resistors 126, 128, and feedback resistors 130, 132. This unity-gain operational amplifier simply provides a delay in the composite differential signal V_{TX} which preferably substantially matches the delay introduced in the replica transmission signals V_{TXR+} and V_{TXR-} by the operational amplifiers 108 and 110. As will be readily appreciated by those of ordinary skill in the art, the various input, output, and feedback resistance values associated with the operational amplifiers 108, 110, and 120 may be selected to ensure that these delays are substantially equal to one another.

[0023] An alternative embodiment of a communications circuit in accordance with the present invention is shown in the schematic diagram of **FIG. 3**. Because the transmission signal replicator 86 and the differential active summer 112 in the embodiment of **FIG. 3** are identical to those in the embodiment of **FIG. 2**, the details of those sub-circuits are

omitted from the description of the embodiment of **FIG. 3**. The embodiment of **FIG. 3**, however, differs from the embodiment of **FIG. 2** in the structure of the sub-circuit provided for converting the single-ended replica transmission signals V_{TXR+} and V_{TXR-} into a differential replica transmission signal V_{TXR}.

[0024] More particularly, as shown in **FIG. 3**, a converter circuit 140 is coupled to the transmission signal replicator 86 and to the differential active summer 112 to produce the differential replica transmission signal V_{TXR} from the single-ended replica transmission signals V_{TXR+} and V_{TXR-}. Just as in the embodiment of **FIG. 2**, the embodiment of **FIG. 3** includes a unity-gain differential operational amplifier 150, which provides a delay in the differential composite signal V_{TX} to substantially match the delay introduced in the differential replica transmission signal V_{TXR} by the converter circuit 140. As will be appreciated by those of ordinary skill in the art, the differential operational amplifier 150 is preferably provided with input, output, and feedback resistors having resistance values which give the differential operational amplifier 150 a unity-gain value. Accordingly, the differential active summer 112 receives as input the delayed differential composite signal V_{TX} and the delayed differential replica transmission signal V_{TXR} and subtracts the latter signal from the former to produce at an output of the differential active summer 112 a differential receive signal which comprises the composite differential signal minus the differential replica transmission signal and thus corresponds to the signal received by the transceiver 70.

[0025] The simplification of the converter circuit 140 in the embodiment of **FIG. 3**, compared to the converter circuit 107 in the embodiment of **FIG. 2**, is made possible by the fact that the single-ended replica transmission signals V_{TXR+} and V_{TXR-} produced by the transmission signal replicator 86 in the illustrated embodiment are characterized by the feature that when V_{TXR+} is asserted then V_{TXR-} is zero (or ground), and when V_{TXR-} is asserted then V_{TXR+} is zero (or ground). It is because the single-ended replica transmission signals V_{TXR+} and V_{TXR-} have this characteristic that the two differential operational amplifiers 108 and 110 of the converter circuit 107 in the embodiment of **FIG. 2** can be replaced by the single differential operational amplifier 142 in the converter circuit 140 of the embodiment of **FIG. 3**.

[0026] This reduction in components in the converter circuit 140 provides not only substantial simplification of the integrated circuit 70 as a whole, but it also reduces the well-recognized manufacturing problem of component mismatch, such as between the two differential operational amplifiers 108 and 110 of the embodiment of **FIG. 2**, for example, and improves common-mode rejection, which, in turn, results in overall improved performance of the transceiver 42.

[0027] The foregoing description is for the purpose of teaching those skilled in the art the best mode of carrying out the invention and is to be construed as illustrative only. Numerous modifications and alternative embodiments of the invention will be apparent to those skilled in the art in view of this description, and the details of the disclosed

structure may be varied substantially without departing from the spirit of the invention. Accordingly, the exclusive use of all modifications within the scope of the appended claims is reserved.